REMARKS/ARGUMENT

Responsive to the rejection of claims 9-14 and 21-22, claims 9-12 have been amended. It is believed that claims 9-14 and 21-22 now comply with Section 112, second paragraph. Reconsideration is requested.

Claims 13 and 14 have been amended to correct an obvious typographical error. The respective scope of each of these claims has not been varied by the amendments. Entry of the amendments is requested.

The rejection of claims 9-14 and 21-22 under 35 U.S.C. §103(a) over Davies, U.S. Patent No. 5,155,052 in view of Ajit et al., U.S. Patent No. 5,474,946 has been maintained.

In the response to the previous Office Action it was argued that Davies requires the use of sidewall spacers when implanting second base diffusions; whereas, in the present invention stripes of oxide and polysilicon are used as a mask for implanting and diffusing dopants to form the second base diffusions.

In paragraph 7 of the Office Action, it was set forth that the claimed invention does not reflect the argument; namely that, sidewall spacers are not used as part of a mask. Claim 9 has been amended to specifically set out that "said stripes of oxide and polysilicon do not include sidewalls during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions." This amendment to claim 9 sets out specifically that which was inherent in the previous recitation. It is respectfully submitted that it is now clear that the subject matter of claim 9 is not shown or suggested by the art of record. Reconsideration is requested.

Claims 10-14 and 21-22 depend from claim 9, and, therefore, include its limitations. Each of these claims includes other limitations, which in combination with those of claim 9, are not shown or suggested by the art of record. Reconsideration of claims 10-14 and 21-22 is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231, on December 11, 2002

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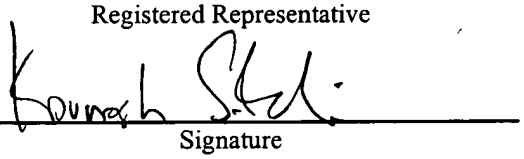

Signature

December 11, 2002

Date of Signature

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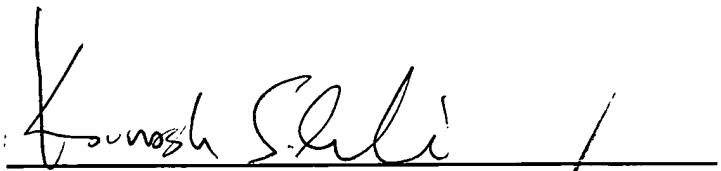
Respectfully submitted,



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APPENDIX B

VERSION WITH MARKINGS TO SHOW CHANGES MADE
37 C.F.R. § 1.121(b)(iii) AND (c)(ii)

CLAIMS:

9. (Four Times Amended) The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said [oxide] silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes[,] into said silicon surface[,] using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base [diffusions] diffusion stripes, said source diffusions, and said second base diffusions [are formed at substantially the same depth].

10. (Amended) The process of claim 9, wherein said polysilicon stripes have a width of [about] 3.1 microns and a spacing of [about] 1.25 microns.

11. (Amended) The process of claim 9 wherein said first base diffusions have a depth of [about] 1.25 microns and said source diffusions have a depth of [about] 0.4 microns.

12. (Amended) The process of claim 10 wherein said first base diffusions have a depth of [about] 1.25 microns and said source diffusions have a depth of [about] 0.4 microns.

13. (Amended) The process of claim 9 which further includes the formation of insulation spacer layers over the [type] top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter

depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. (Amended) The process of claim 12 which further includes the formation of insulation spacer layers over the [type] top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

APPENDIX C
complete set of "clean" claims
pursuant to 37 C.F.R. §1.121(c)(3)

9. The process of manufacture of a MOSgated device comprising:

forming a gate oxide layer atop a silicon surface of one conductivity type;

forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and said underlying gate oxide layer into a plurality of stripes of oxide and polysilicon spaced 1 to 4 microns and overlying said silicon surface; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of oxide and polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of oxide and polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; implanting and diffusing second base diffusion stripes into said silicon surface using said stripes of oxide and polysilicon as a mask, to a depth below that of said source diffusions and extending to between the opposite edges of adjacent pairs of said polysilicon stripes; wherein said stripes of oxide and polysilicon do not include sidewall spacers during implanting and diffusing of said first base diffusion stripes, said source diffusions, and said second base diffusions.

10. The process of claim 9, wherein said polysilicon stripes have a width of 3.1 microns and a spacing of 1.25 microns.

11. The process of claim 9 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

12. The process of claim 10 wherein said first base diffusions have a depth of 1.25 microns and said source diffusions have a depth of 0.4 microns.

13. The process of claim 9 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. The process of claim 12 which further includes the formation of insulation spacer layers over the top and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

21. The process of claim 9 wherein said polysilicon stripes are spaced 1.5 microns apart.

22. The process of claim 9 wherein said polysilicon stripes are spaced 3.2 to 3.4 microns wide.